UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,812	09/25/2003	Claire Richtarch	4717-11300	6886

28765 7590 08/09/2005

WINSTON & STRAWN LLP
1700 K STREET, N.W.
WASHINGTON, DC 20006

EXAMINER	
LINDSAY JR, WALTER LEE	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,812	RICHTARCH, CLAIRE	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5 and 15* is/are allowed.

6)☒ Claim(s) *1,3,4,6-14 and 16-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an Amendment filed 5/19/2005.

Currently, claims 1 and 3-20 are pending.

Specification

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1, 4, 10-14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Augustine et al. (U.S. Patent No. 5,895,583 dated 4/20/1999) in view of Ueno (U.S. Patent No. 6,136,727 dated 10/24/2000) and Yamada et al. (U.S. Publication No. 2005/0042800 filed 1/10/2003).

Augustine shows the method substantially as claimed in Figs. 1-5C and corresponding text as: polishing the conditioned SiC surface of the wafer (40) with an abrasive in order to provide a wafer surface that is suitable for growing an epitaxial layer thereon (col. 3, lines 30-45) (claim 1). Augustine teaches that the polishing is conducted with a polishing head that is rotated at about 10 rpm to about 100 rpm (col. 4, lines 6-16) (claim 11). Augustine teaches that a pressure of about 0.1 bar to about 1 bar is applied to the polishing head during rotation (col. 4, lines 23-32) (claim 12). Augustine teaches that the wafer surface is polished for about 15 minutes to about 30 minutes (col. 4, lines 45-51) (claim 13). Augustine teaches that the polishing is conducted with an IC1000 type polishing pad (col. 4, lines 33-44) (claim 14). Augustine teaches that the polishing is conducted to provide a surface roughness of less than 15 angstroms RMS (col. 4, lines 52-58).

Augustine lacks the anticipation of explicitly teaching that: 1) annealing the wafer in an oxidizing atmosphere to condition the SiC surface (claim 1); and 2) the annealing is conducted at a temperature of about 1000°C to about 1300°C (claim 4).

Ueno forms a silicon carbide device in an oxidizing atmosphere. The SiC wafer is inserted into an oxidizing furnace and then heated to 1100°C (col. 4, lines 52-63). This process is to increase the value of channel mobility an important characteristics of a semiconductor device having excellent characteristics (col. 2, line 65-col. 3, line 3).

It would be obvious to one of ordinary skill in the art, at the time the invention was made, to modify the method of Augustine by annealing the wafer in an oxidizing atmosphere to condition the SiC at a temperature of about 1000°C to about 1300°C, as

taught by Ueno, with the motivation that Ueno teaches that by implementing the oxidation the value of channel mobility is increased.

Augustine as modified by Ueno lacks anticipation of explicitly teaching that: 1) treating the wafer surface to reduce surface roughness; and polishing the treated and conditioned SiC surface of the wafer with an abrasive based on particles of colloidal silica in order to provide a wafer surface that is suitable for growing an epitaxial layer thereon (claim 1); and 2) the colloidal silica particles used for polishing the wafer surface include Syton W30 type colloidal silica (claim 10).

Yamada shows the production of SiC wafers. Yamada polishes the SiC wafer with colloidal silica as an abrasive material, pH of the slurry between 10 to 11 [0027]. Syton W30 type colloidal silica is a well-known, form of colloidal silica [0027]. This helps to produce a SiC wafer having an ultra-flat and clean surface at low cost [0008].

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Augustine as modified by Ueno by polishing the SiC with colloidal silica, as taught by Yamada, with the motivation that Yamada that, colloidal silica aids the production of SiC wafer having an ultra-flat and clean surface at low cost.

5. Claims 3, 16 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Augustine et al. (U.S. Patent No. 5,895,583 dated 4/20/1999) in view of Ueno (U.S. Patent No. 6,136,727 dated 10/24/2000) and Yamada et al. (U.S. Publication No. 2005/0042800 filed 1/10/2003) as applied to claim 1 above, and further in view of Goesele et al. (U.S. Patent No. 5,877,070 dated 3/2/1999).

Augustine as modified by Ueno and Yamada lack anticipation of explicitly teaching that: 1) the SiC surface layer is bonded to a semiconductor substrate (claim 3); 2) the polishing is conducted to make the wafer surface suitable for homoepitaxy or heteroepitaxy (claim 16); 3) an epitaxial layer is deposited upon the polished wafer surface (claim 18); and 4) the epitaxial layer comprises at least one of SiC, AlN, GaN or AlGaN (claim 19).

Goesele teaches the formation of a silicon carbide substrate (col. 11, lines 39-48). Then a gallium nitride epitaxial layer is then bonded to the silicon carbide substrate (col. 12, lines 25-39). The process has the essentially flat and mirror polished silicon carbide and bonding it to a flat and mirror polished gallium nitride (col. 3, lines 46-50). The process allows for several thin layers to be formed from the same substrate (col. 1, lines 6-15).

It would be obvious to one of ordinary skill in the art, at the time the invention was made, to modify Augustine as modified by Ueno and Yamada by bonding and growing an epitaxial layer on the SiC that is either homoepitaxy or heteroepitaxy and consist of a layer from the group of SiC, AlN, GaN or AlGaN, as taught by Goesele with the motivation that Goesele teaches that several thin layers can be formed from the same substrate.

6. Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Augustine et al. (U.S. Patent No. 5,895,583 dated 4/20/1999) in view of Ueno (U.S. Patent No. 6,136,727 dated 10/24/2000) and Yamada et al. (U.S. Publication No.

2005/0042800 filed 1/10/2003) as applied to claim 1 above, and further in view of Tanimoto et al. (U.S. Patent No. 6,833,562 filed 12/2/2002).

Augustine as modified by Ueno and Yamada lack anticipation of explicitly teaching that: 1) the wafer surface is treated by a deoxidizing step or by applying an RCA (SC1, SC2) type chemical cleaning step prior to polishing (claim 6); 2) the wafer surface is deoxidized with hydrofluoric acid (claim 7); 3) chemically cleaning the wafer surface (claim 8); and the wafer surface is cleaned with hydrofluoric acid (claim 9).

Tanimoto shows the cleaning of a SiC substrate. The substrate is sufficiently washed by RCA cleaning. Thereafter the substrate is immediately immersed in hydrofluoric acid buffer solution so as to remove the thermal oxide films (col. 10, line 59-col. 11, line 12). The cleaning process reduces causes of a thermal loss and of operating speed reduction and to form high performance gate insulating film (col. 1, lines 43-53).

It would be obvious to one of ordinary skill in the art, at the time the invention was made, to modify Augustine as modified by Ueno and Yamada by cleaning the substrate through a RCA step followed by hydrofluoric acid, as taught by Tanimoto, with the motivation that Tanimoto teaches that the cleaning process reduces causes of thermal loss and operating speed reduction and to form high performance gate insulating film.

Response to Arguments

7. Applicant's arguments filed 5/19/2005 in Application No. 10/671812 have been fully considered but they are not persuasive. The examiner uses Augustine as the basis of this rejection and as the Applicant has noted Augustine speaks to the core teaching

of what is claimed. The issue of time, which is raised by the Applicant in this regard, is not found in the base teaching of claim 1 but is found in claim 5, which was indicated to be allowable subject matter in the previous Office Action. The examiner uses Ueno to remedy the deficiencies found in Augustine, Applicant points out that Ueno does teach a shorten preparation time or how to prepare an epiready film, the examiner would like to point out that Ueno is use to teach an oxidation step and as the claims are written in present form this is the only limitation that needs to be addressed by Ueno, the present claims do not deal with preparation time as written. Gosele teaches the bonding of layers to silicon carbide and Tanimoto teaches cleaning a silicon carbide substrate with RCA cleaning, the surface used by both is silicon carbide. The core of the rejection is the handling of silicon carbide of which is consistently dealt with in the prior art.

8. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, silicon carbide is the constant medium on which these processes are carried out. In response to applicant's arguments, the recitation "preparing a SiC surface of a semiconductor wafer to make it epiready" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it

merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

9. Applicant's arguments with respect to claims 1, 3-4, 6-14, and 16-19 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

10. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. Claims 5 and 15 are allowed.

1. The following is an examiner's statement of reasons for allowance: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...wherein the annealing is conducted for about 1 hour to about 3 hours, as required by claim 5;

2. ...comprising etching the wafer surface with ions prior to polishing, as required by claim 15; and

...wherein the wafer is annealed under conditions sufficient to produce a surface roughness that is on the order of about 2 nm rms, the conditioned surface is treated to prevent crystallization of abrasive during the polishing step, and the polishing step is

conducted to achieve a surface roughness that is on the order of about 3 Å rms, as required by claim 20.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL
August 5, 2005